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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,153	08/04/2003	Ward D. Parkinson	ITO.0553US (P16341)	5107

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EXAMINER	
NGUYEN, VIET Q	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/634,153	PARKINSON ET AL.	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Application filed on 8/4/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~[illegible]~~ 11/3/04, 10/21/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

VN

DETAILED ACTION

Claims **1-25** are present for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-25** rejected under 35 U.S.C. 103(a) as being unpatentable over **Reinberg et al (6,189,582), Ovshinsky (RE37,259), Gonzalez et al (6,797,978), Gilton (6,809,362),Lung (6,750,101), Zahorik (6,797,612), Klersy et al (5,933,365), and Czubatyj et al (5,825,046).**

Reinberg et al (see Fig.3) clearly shows an analog memory cell using a memory element (30), as programmable resistive element made out of chalcogenide material. Col. 6 (lines 19-33) mentions that "..***chalcogenide resistor is made of a state changeable material that can be switched from one detectable state to another detectable state or states***...", thus obviously suggests that this memory element is "***phase change material***" and it can be used to stored either digital data (i.e, as distinct states) or analog data (i.e., as different resistances

measured). Col. 6 (lines 34-42) further stated that "...the resistance of an exemplanary chalcogenide resistor as a function of voltage applied across the resistor", thus also obviously suggests that the resistance values are also variable and programmable as recited.

In regard to the claimed "programming current", col. 7 (lines17-18) mentions the magnitude of current pulse will determine the programmed resistance value to be stored thus obviously enabling the resistance to be read and readjust as desired.

Ovshinsky (see Fig. 1) shows an analog memory cell comprising a phase change material (36, chalcogenide), see also col. 13 description) that can be programmed with variable resistance values. Col. 4 (lines 27-39) also mentions the range of resistance is varied and programmable in different states thus obviously suggest that the memory element can store either analog or digital data values. See al so cols. 7-12.

Gonzalez et al (see Fig. 1) shows an analog memory cell comprising a phase change material (5, chalcogenide), see also col. 2 description, that can be programmed with variable resistance values. Col. 2 (lines 27-39) also mentions the range of resistance is varied and programmable in different states thus obviously suggest that the memory element can store multi-bit values as either analog or digital data.

In regard to the claimed "pore", col. 2 also mentions the desired pore size to be used. See al so cols. 4-7.

Gilton (see Fig.1) shows an analog memory cell comprising a phase change material (layer 204, chalcogenide), that can be programmed with variable resistance values. Col. 4 also mentions the range of resistance is varied and programmable in different states thus obviously suggest that the memory element can store multi-bit values as either analog or digital data. See also cols. 3-5.

Lung (see Fig. 1) shows an analog memory array using phase change material, and col. 3 mentions that "the phase change material can be adapted to store more than one bit by assuming more than two bulk resistance states in response to programming current or other programming stimulus", thus obviously suggest that the memory element can store multi-bit values as either analog or digital data. See also cols. 3-5.

Zahorik (see Fig. 4) shows an analog memory using a phase change material and Fig. 6 shows an opening (110) defining a "pore" in the insulating layer (80) for depositing a phase change material, i.e., chalcogenide (see col. 6), that has various resistance states, thus obviously suggest that the memory element can store multi-bit values as either analog or digital data. See also cols. 7-12.

Klersy et al (see Fig. 1) shows an analog memory using a phase change material (material 36) and shows an opening (36) defining a" pore" in the insulating layer for depositing a phase change material, i.e., chalcogenide (see col. 6), that has various resistance states, thus obviously suggest that the memory element can store multi-bit values as either analog or digital data. See also cols. 12-17.

Czubatyj et al (see Fig. 1) shows an array of analog memory cells, each cell using a phase change material (material 36) and shows an opening (36) defining a "pore" in the insulating layer for depositing a phase change material, i.e., chalcogenide (see col. 6), that has various resistance states, thus obviously suggest that the memory element can store multi-bit values as either analog or digital data. See also cols. 5-13.

Regarding the claimed "circuit" to write analog data, a "processor", and a "wireless interface" etc., or any other devices to be used with these disclosed phase-change memory type, it is noted that all the above references only disclose the use of this phase-change material memory in any computer and/or general memory circuit construction. However, one having ordinary skilled in the art with expertise in the memory technology knows that any type of memory can be coupled with any processor or any I/O, computing devices, and thus it would

have been obvious to these skilled artisans to use these phase-change material memory with any circuit in order to accomplish the necessary data writing and reading if desired.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827

V. Nguyen
4/5/2005